

NOVATECH INSTRUMENTS, INC.

400MHz Programmable Signal Source Model 440A



The Model 440A Programmable Signal Source generates a low distortion sinewave signal from 200kHz to 400MHz with 1Hz resolution. The 440A contains an internal temperature compensated crystal oscillator that can be locked to an external reference in 8kHz steps, allowing the 440A to lock to common telecom signals, such as T1 and E1 rates, as well as common instrumentation frequencies such as 5MHz and 10MHz without external hardware. When locked, the accuracy and stability of the 440A will match that of the reference. The relative phase of the 440A can be controlled with 14-bits of resolution. The 440A is set by sending simple text commands over a 19.2kBaoud serial interface. Four 440A can be mounted in a 1U rack and eight in a 2U rack with optional rack adapters. The 440A operates from a single +5VDC power supply (AC-line adapter provided).

Specifications:

OUTPUT

TYPE: Sine. (optional ECL/TTL)
IMPEDANCE: 50Ω.
RANGE: 200kHz to 400MHz in 1Hz steps.
AMPLITUDE: approximately 0dBm (630mV_{pp} set at 25MHz) into 50Ω.

CONTROL

Output frequency (32-bits) and phase (14-bits) are controlled by sending simple text commands over a bit-serial interface port (RS232) at 19.2kBaoud. Settings can be saved in EEPROM via the serial port.

ACCURACY AND STABILITY

Accuracy: <±1.5ppm at 10 to 40°C. Stable to an additional ±2ppm per year, 18 to 28°C. (Internal Clock)

REFERENCE CLOCK IN

LEVEL: 0.75-2.0Vrms Sine or Square Wave. 50Ω.
FREQUENCY: 1MHz to 25MHz, 8kHz steps. The internal oscillator will track the externally supplied reference as long as the external frequency is within ±5ppm of the nominal value set using the "F_r" command. The default external reference setting is 10.0MHz. When locked the output frequency maintains the accuracy and the stability of the reference clock with no binary round-off to the 1Hz resolution of the "F₀" command. The external reference can be disabled to use the internal oscillator in free-run mode.

SPECTRAL PURITY (Typ. 50Ω load, 10MHz ref.)

Phase Noise: <-120dBc, 10kHz offset, 10MHz output.
Spurious: <-55dBc below 10MHz (typ. 500MHz span)
<-50dBc below 80MHz
<-45dBc below 160MHz
<-35dBc below 400MHz
Harmonic: <-60dBc below 1MHz
<-55dBc below 20MHz
<-50dBc below 80MHz
<-40dBc below 160MHz
<-35dBc below 400MHz

POWER REQUIREMENTS

+5VDC (+4.75 to +5.25) @<1.0A. (90-240VAC with provided AC-adapter)

SIZE

39mm H, 107mm W, 172mm L, not including connectors.

ENVIRONMENTAL

Temperature: 0°C to +50°C operating.
Humidity: 80% to 31°C, decreasing linearly to 50% at 40°C.

CONNECTORS

Sine: front panel SMA; Reference In: rear panel BNC.
RS232 control: DE9F on rear panel. +5V DC Power: 2.5mm power receptacle, center positive.

14-Jun-2011

Serial Commands

RS232 Command	Function
F0 xxx .xxxxxxx	Set Frequency Zero in MHz to nearest 1Hz. Decimal point required. Maximum 'F0' setting is 402.653183MHz
Fr xx .xxx	Sets the Reference Frequency in MHz in 8kHz steps. Decimal point required. Range: 1MHz to 25MHz. This value is used to phase lock the internal master clock to the externally supplied clock. Software rounds down to lowest 8kHz multiple.
P0 N	Set Phase Zero. N is an integer from 0 to 16383. Phase is set to $N*360/16384$ degrees ($N*\pi/8192$ radians). This command sets the relative phase of the output sine wave. This is useful for adjusting the phase of the output after the 440A has obtained lock. Factory default is N=0.
C x	Enable (x=E) or Disable (x=D) external lock. When disabled, the internal TCXO is used without locking to an externally supplied clock.
E x	Serial Echo Control. x=D for Echo D isable, x=E for Echo E nable. Default is E nabled.
T x	ECL Output Control. x=D for ECL D isable, x=E for ECL E nable. Default is D isabled. (requires internal configuration)
S	Save current state into EEPROM and sets the EEPROM valid flag. The state saved is used as default upon next power up or reset.
STOP	Turns off the internal microprocessor. The "STOP" command automatically saves all present settings. Use this command in embedded applications for lowest system noise and power. A logic low (open collector) pulse must be applied to the CLR_STOP* connector pin to restore normal operation. After a CLR_STOP* pulse, factory defaults are restored. (an internal on-board push button implements the "CLR_STOP*" pulse)
R	Reset. This command resets the unit. EEPROM data is preserved and, if valid, it is used upon restart. This is the same as cycling power or toggling the open collector RES* line on the connector. (an internal on-board push button implements a "RES*" pulse)
CLR	Clear. This command clears the EEPROM valid flag and restores all factory default values.
QUE	Read present frequency, phase and status. Returns a character string of internal settings, lock status and software revision number. Hexadecimal format. See operating notes for details.

P1 Header Pinout (LPO400A only)

Pin Number	Function	Type	Pin Number	Function	Type
1	Ground (Power Supply Common)	PS	2	NC (open: for LPO30A compatibility)	-
3	TX, serial ASCII data FROM module, TTL level (3.3 V CMOS)	Out	4	Ground (Power Supply Common)	PS
5	NC (open: for LPO30A compatibility)	-	6	RX, serial ASCII data TO module, TTL level (3.3 V CMOS)	In
7	+3.3 VDC <i>INPUT</i>	PS	8	RES*, Open Collector Reset Pin, normally left open.	In
9	Ground (Power Supply Common)	PS	10	CLR_STOP*, Open Collector Input Pin. Pulsing low clears module to factory default outputs and settings.	In
11	INLOCK (TTL level, 3.3 V CMOS),	Out	12	Ground (Power Supply Common)	PS
13	RF_IN, Reference Clock Input, 50Ω.	In	14	Ground (Power Supply Common)	PS

Operating Notes for assembly LPO400A/440A, with REV 1.x Software.

(August 23, 2005)

1: The 'QUE' command has been rewritten to provide data specific to the LPO400A. The command returns a thirty-three character ASCII string terminated by a CRLF. Values are in Hexadecimal:

0000 02625A00 2710 00000078 03 10

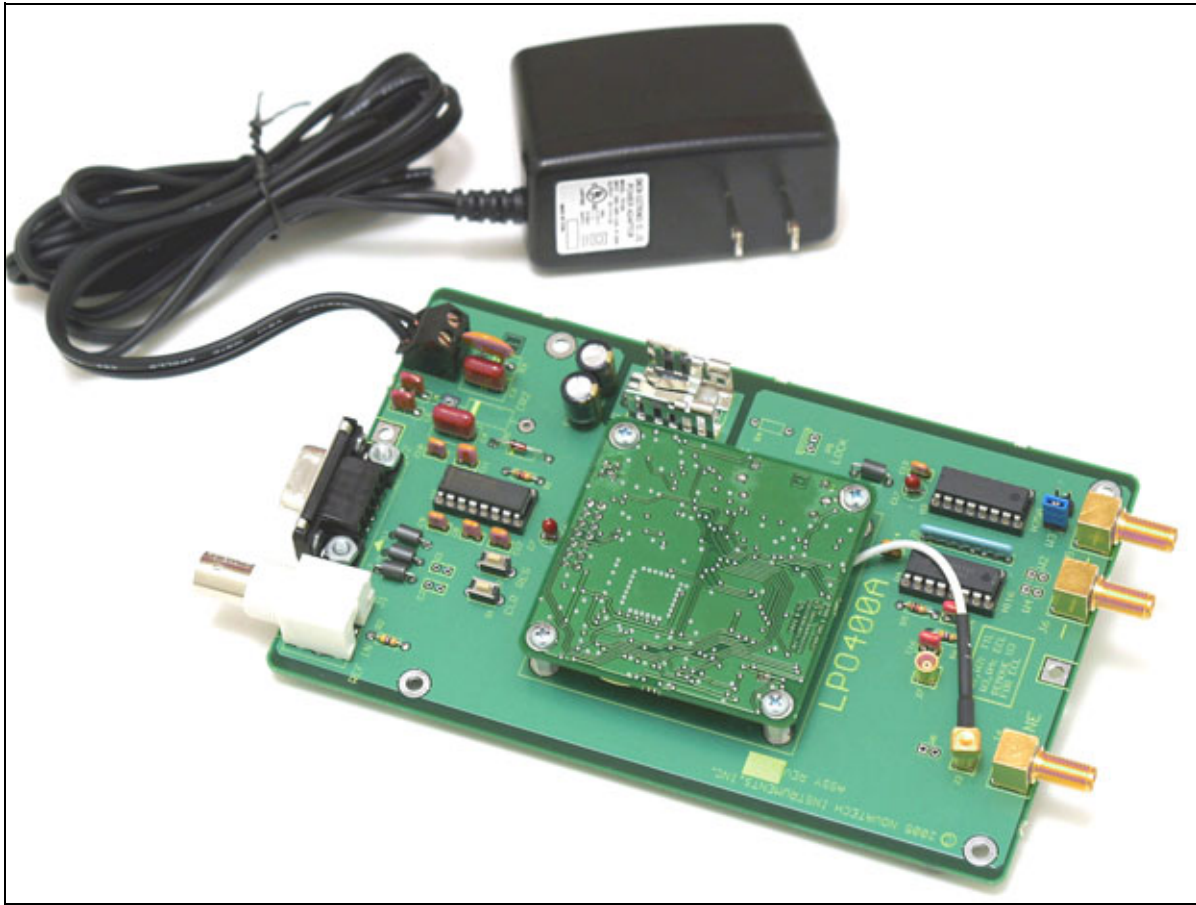
Decoding:

0000	Relative phase in Hex. Maximum value of '3fff'. Set by "P0" command.
02625A00	32-bit Frequency data (4-bytes), as hexadecimal. This value is the frequency in 0.25Hz steps. 10.0MHz default value. Set by "F0" command
2710	Reference frequency set by 'Fr' command. Software sets to lowest 8kHz boundary. Saved as a hex value as kHz. 10000 (as hexadecimal), for 10MHz reference frequency, default.
00000078	Control Register values. These are internal setup values.
03	This byte contains status bits. The LSB is the lock bit. If an out-of-lock condition is detected, the bit will go low (even). '03' means that the LPO400A has been locked. The on-board microcomputer reads the lock pin every millisecond and sets this value low upon detection of a out-of-lock. Approximately one minute is required for complete lock detection.
10	Software revision as 'x.x' or Rev 1.0 for this example.

2: The InLock Pin on the interface connector, pin 11 of P1, will be steady logic high during lock. During the locking process, this pin may be erratic. It is suggested that, if you use this pin, it be polled. The on-board microprocessor reads the lock status each millisecond and requires 2^{16} in-lock levels in a row for lock detection (approximately one minute). The lock detect process cannot detect minor changes in the reference input or the lock frequency setting ($>\pm 100$ ppm error may still indicate lock). This pin is not accessible on the Model 440A. On the 440A, the lock condition is indicated by the front panel LED. When illuminated GREEN, the unit is in lock, or using internal clock. When illuminated RED the unit is out of lock (missing external reference, or internal failure).

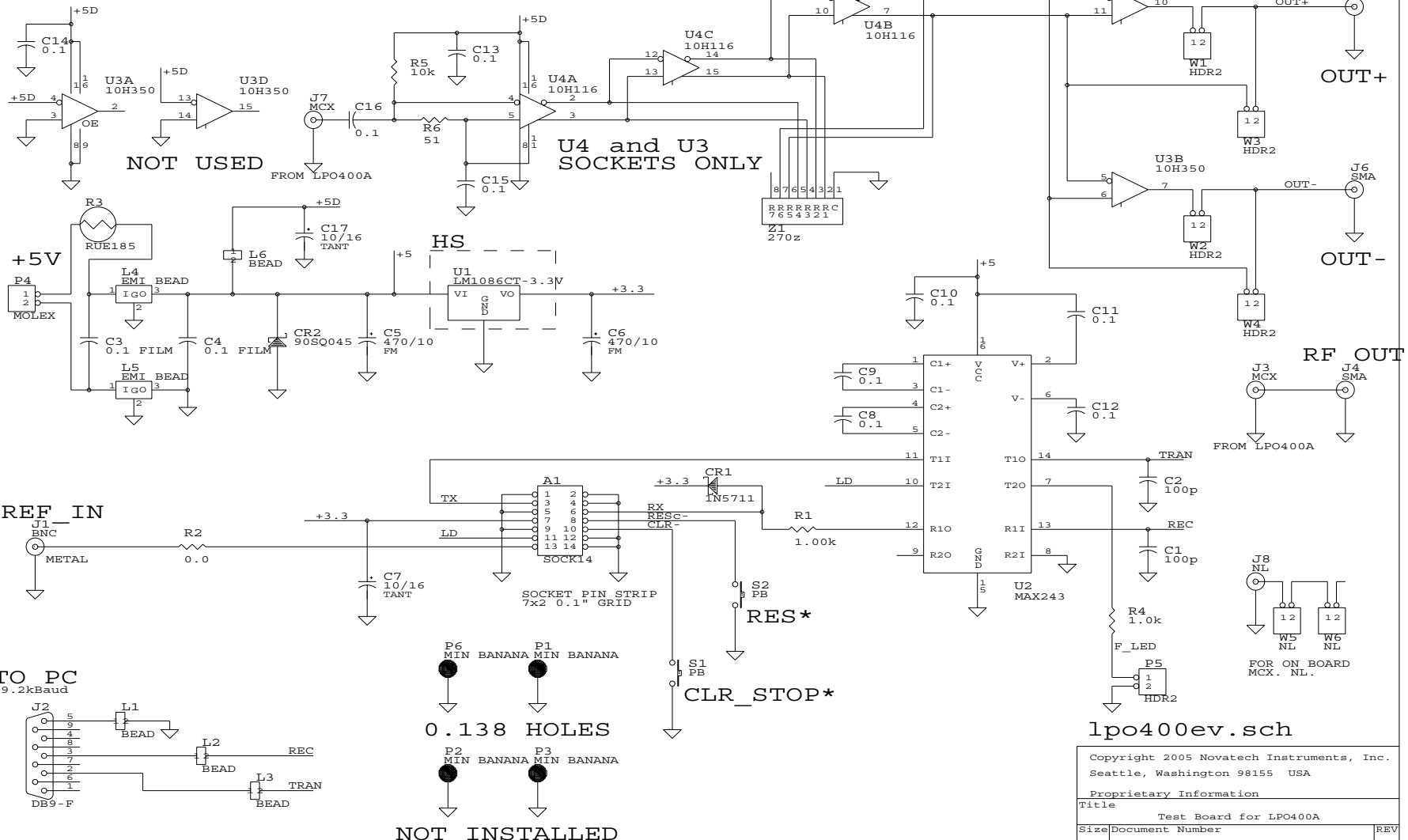
3: Commands return 'OK' if parsed and executed correctly.

4: The on board green LED is illuminated when both on-board loops are in "Lock," or the external reference has been disabled. If the LED is not illuminated, then a lock error is indicated. See 2 (above) for front panel LED indications for the Model 440A.



The LPO400A evaluation board is similar to the 440A, but is supplied without a case to make evaluation of the LPO400A module easier. See the schematic below for details on the board.

LPO400A TEST INTERFACE FIXTURE



lpo400ev.sch

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Proprietary Information

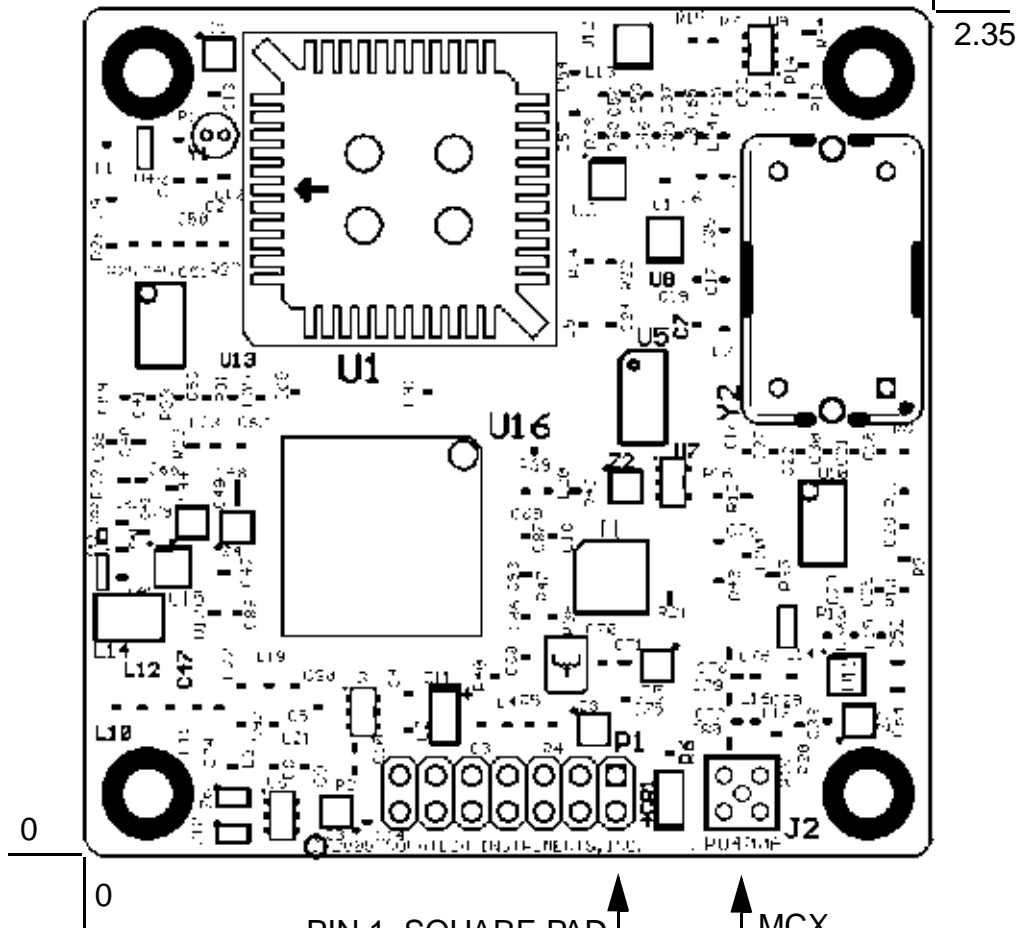
Title: Test Board for LPO400A

Size	Document Number	REV
B		A

Date: August 4, 2005 Sheet 1 of 1

LPO400A, COMPONENT SIDE VIEW

2.35



PIN 1, SQUARE PAD,
(1.475,0.225)

MCX,
JOHNSON COMPONENTS
133-3701-133
(1.825,0.175)

Mounting Holes at:
(0.175,0.175), (2.175,0.175),
(2.175,2.175), (0.175,2.175)

P1 two rows by seven pos.,
on 0.1 (2.54mm) grid.

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NOVATECH INSTRUMENTS, INC.

P.O. Box 55997
Seattle, Washington 98155-0997
United States of America

FAX: 206.363.4367
TEL: 206.301.8986
<http://www.novatech-instr.com>
sales@novatech-instr.com

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