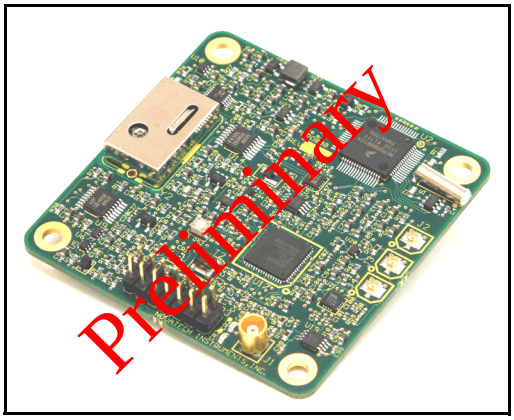
NOVATECH
INSTRUMENTS, INC.

800 MHz Locking Programmable Oscillator Module

Model LPO800A



The LPO800A is a Direct Digital Synthesized Locking Programmable Oscillator on a 60 mm square circuit board module. The LPO800A generates differential CML to 800 MHz, Sine to 400 MHz and LVCMOS to 100 MHz. The serial interface uses simple text commands to control the module and allows non-volatile storage of all settings. The LPO800A is equipped with a ±1.5 ppm on-board VCTCXO clock, which can be locked to a external frequency standard, or used independently. Requiring only a single +3.3 V power source, the LPO800A is ideal for embedded applications which require programmable frequency sources or for replacing long-lead time custom oscillators. The LPO800A can be used as an upgrade for the LPO30A or for the LPO400A. An LPO800A evaluation board contains serial drivers, AC-adapter power supply, connectors and software for simplified testing and programming.

Specifications:

CML:

AC-Coupled: terminate to 50 Ω single-ended or 100 Ω differential output. Can be used single-ended. V_o > 320 mV_{pp}, $T_{r,f}$ <350 ps (20-80%), when terminated. Internal doubler provides operation to 800 MHz. Frequency equals Sine output unless doubler is enabled.

SINE:

IMPEDANCE: 50Ω.
RANGE: 200 kHz to 400 MHz in 0.01 Hz steps.
SINE AMPLITUDE: approximately 0 dBm (630 mV_{pp} ±30 mV_{pp} set at 25 MHz) into 50 Ω, ±3 dB from 100 MHz level.

LVCMOS:

V_{OL}<0.5 V, V_{OH}>2.0 V into a series-terminated load, $T_{r,f}$ <2.5 ns. 50 Ω. Programmable 16-bit divider with a selectable /2 prescaler allows LVCMOS frequencies below 2 Hz. (LVCMOS optimized for <= 100 MHz). Same frequency as Sine output unless divider or /2 is enabled.

CONTROL

Output settings are controlled by a bit-serial asynchronous port (RS232 at TTL/CMOS levels) at 19.2 kBaud. Settings can be saved in EEPROM.

ACCURACY AND STABILITY

Accuracy: <±1.5ppm at 10 to 40°C. Stable to an additional ±2ppm per year, 18 to 28°C. (Internal Clock)

REFERENCE CLOCK IN

LEVEL: 0.5-2.0 Vrms Sine or Square Wave. 50 Ω.
FREQUENCY: 1 MHz to 16 MHz, in 1 MHz steps. The on-board voltage-controlled temperature compensated crystal oscillator (VCTCXO) will track the externally supplied reference frequency a minimum ±5 ppm from the nominal value set using the `"Fr"` command. Default reference setting is 10.000 MHz. When locked, the output frequency maintains the accuracy and the stability of the reference clock with no binary round-off.

SPECTRAL PURITY (Sine, Typ. 50 Ω load, 10 MHz ref.)

Phase Noise:	<-140 dBc, 10 kHz offset, 10 MHz out.
Spurious:	<-70 dBc below 10 MHz
	<-65 dBc below 50 MHz
	<-55 dBc below 150 MHz
	<-40 dBc below 400 MHz
Harmonic:	<-65 dBc below 1 MHz
	<-60 dBc below 10 MHz
	<-55 dBc below 25 MHz
	<-45 dBc below 50 MHz
	<-40 dBc below 150 MHz
	<-20 dBc below 400 MHz

POWER REQUIREMENTS

3.15 to 3.45 V@<750 mA (+3.3 VDC ±5%)

SIZE

60 mm by 60 mm circuit board. Max. height 10 mm.

CONNECTORS

MCX for Sine output, Two UMC for differential CML output and a single UMC for LVCMOS. 14-pin header for power, reference clock and control signals.

ACCESSORY

LPO800A-EVAL board kit contains AC-adapter, Serial drivers, PC serial cable and SMA connectors for evaluation and programming of the LPO800A module. SOF8 software included with LPO800A-EVAL.

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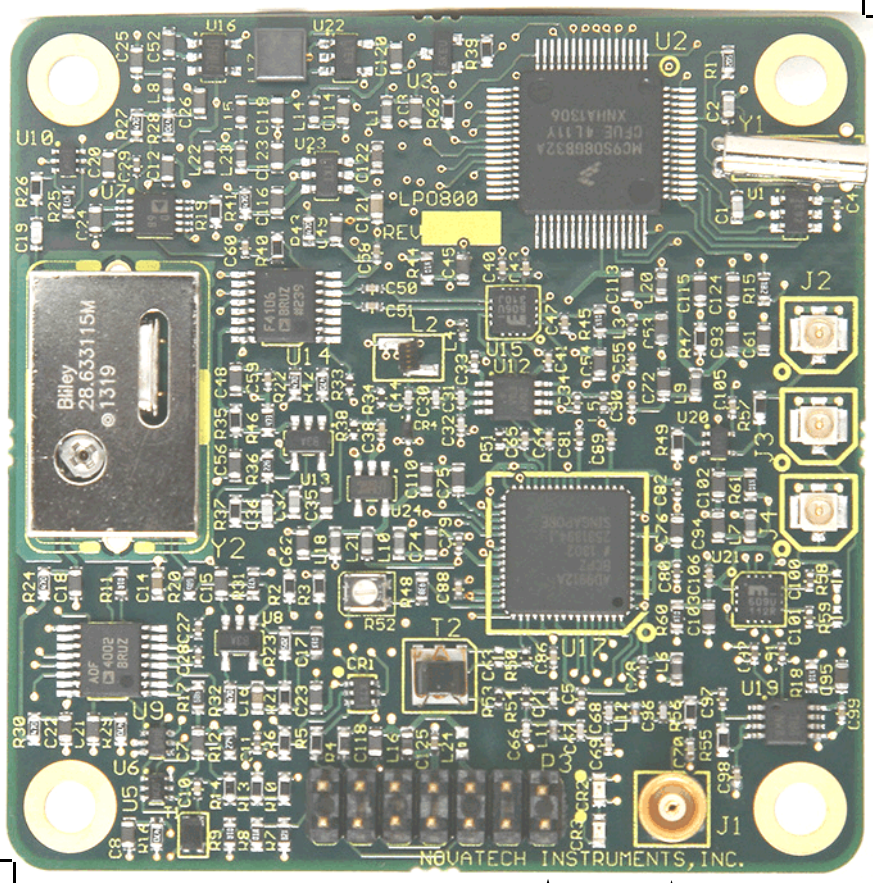
LPO800A Serial Commands

Serial Command	Function
F0 xxx.xxxxxxxx	Set Sine Output Frequency in MHz with exact 0.01 Hz resolution. Decimal point required. Default output is 10.000 MHz.
Fr xx	Sets the Reference Frequency in MHz. Range: 1 to 16 MHz. This value is used to phase lock the internal master clock to the externally supplied clock. The supplied reference must be within ±5 ppm the value set by this command. Default value is 10.000 MHz.
P0 N	Set Phase. N is an integer from 0 to 16383. Phase is set to N*360/16384 degrees or N*π/8192 radians. Sets the relative phase of the output sine wave. This is useful for adjusting the relative phase of the output after the LPO800A has obtained lock. Factory default is 0.
C x	**E**nable (x=E) or **D**isable (x=D) external lock. When disabled, the internal VCTCXO is used without locking to an externally supplied clock. Default is "E." "C E" uses last reference value.
E x	Serial Echo Control. x=D for Echo **D**isable, x=E for Echo **E**nable. Default is **E**nabled.
A x	CMOS Output Control. x=D for **D**isable, x=E for **E**nable. Default is **D**isabled.
H x	**H**igh Speed output. Enable (x=E) changes the CML output to the high speed path at double the Sine output frequency. Usable from 400 MHz to 800 MHz (Sine output, "F0", from 200 to 400). x=D disables the high speed path and reverts the CML to the sine frequency. Default is "D."
S	Save current state into EEPROM and sets the EEPROM valid flag. The state saved is used as default upon next power up or reset.
D0 N	Set **D**ivider value on LVCMOS output. N is an integer from 0 to 65535. The output frequency set by the "F0" command is divided by N+1 before being sent to the LVCMOS driver. Duty cycle varies with divide ratio. Default is "0."
PR x	x=E for Enable **Pr**escaler, x=D for Disable Prescaler. When enabled, the frequency set by the "F0" command is divided by 2 before entering the LVCMOS divider specified by the "D0" command. This allows a maximum divide integer of 131072. Default is "D."
R	Reset. This command resets the unit. EEPROM data is preserved and, if valid, it is used upon restart. This is the same as cycling power or toggling the open collector RES* line on the connector.
CLR	Clear. This command clears the EEPROM valid flag and restores all factory default values.
QUE	Returns a character string of output settings, internal settings, lock status and software revision number. Hexadecimal format. See manual for details.

Control Connector Pinout

Pin Number	Function	Type	Pin Number	Function	Type
1	Ground (Power Supply Common)	PS	2	NC (do not connect)	-
3	TX, serial ASCII data FROM module, TTL level (3.3 V CMOS)	Out	4	Ground (Power Supply Common)	PS
5	NC (open: for LPO30A compatibility)	-	6	RX, serial ASCII data TO module, TTL level (3.3 V CMOS)	In
7	+3.3 VDC ***INPUT***	PS	8	RES*, Open Collector Reset Pin, normally left open.	In
9	Ground (Power Supply Common)	PS	10	CLR_STOP*, Open Collector Input Pin. Pulsing low clears module to factory default outputs and settings.	In
11	INLOCK (TTL level, 3.3 V CMOS),	Out	12	Ground (Power Supply Common)	PS
13	RF_IN, Reference Clock Input, 50Ω.	In	14	Ground (Power Supply Common)	PS

LPO800A, COMPONENT SIDE VIEW



ACMOS OUT
(2.225,1.475)

CML- OUT
(2.225,1.225)

CML+ OUT
(2.225,0.975)

AMC/UMC,
Molex,
0734120110,
or equiv.

PIN 1, SQUARE PAD,
(1.475,0.225), P1.

MCX,
JOHNSON COMPONENTS
133-3701-133, or equiv.
(1.825,0.175)
SINE OUTPUT

Mounting Holes at:
(0.175,0.175), (2.175,0.175),
(2.175,2.175), (0.175,2.175).
Connected to circuit common (ground).

P1 two rows by seven pos.,
on 0.1 (2.54mm) grid. FCI
Dubox #68683-307 or Amp
#534998-7.